TSMC-01-427

February 9, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/726,105 12/02/03

Ta-Lee Yu

IMPROVED SCR-ESD STRUCTURES WITH SHALLOW TRENCH ISOLATION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 2/17/04

U.S. Patent 6,172,403 to Chen, "Electrostatic Discharge Protection Circuit Triggered by Floating-Base Transistor," discloses an ESD circuit with a process involving AA, isolation areas, and silicide.

U.S. Patent 5,012,317 to Rountre, "Electrostatic Discharge Protection Circuit," discloses a conventional SCR-ESD circuit protection device with parasitic bipolar transistors.

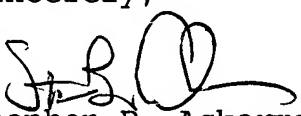
U.S. Patent 5,629,544 to Voldman et al., "Semiconductor Diode with Silicide Films and Trench Isolation," discusses a diode in a well having trench isolation that has an edge.

U.S. Patent 6,236,087 to Daly et al., "SCR Cell for Electrical Overstress Protection of Electronic Circuits," discloses an input protection device for protecting a circuit structure which is coupled to a first node, the device comprising a first lightly-doped region of P-type material with a lightly doped well on N-type material formed in it.

U.S. Patent 5,903,424 to Tailliet, "Method for Protecting an Integrated Circuit Against Electro-Static Discharges," discloses a device for the protection of integrated circuits against electrostatic discharges.

U.S. Patent 5,530,612 to Maloney, "Electrostatic Discharge Protection Circuits Using Biased and Terminated PNP Transistor Chains," discloses a device requiring ESD protection where a bias network is used to augment the diode string to distribute small but significant forward current to the diodes.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-427B	10/726,105
Applicant: Ta-Lee Yu	
Filing Date: 12/02/03	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6172403	1/9/01	Chen	257	355	12/15/98
	5012317	4/30/91	Rountre	357	38	6/27/88
	5629544	5/13/97	Voldman et al.	257	355	4/25/95
	6236087	5/22/01	Daly et al.	257	355	11/2/98
	5903424	5/11/99	Tailliet	361	111	12/2/96
	5530612	6/25/96	Maloney	361	56	3/28/94

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.